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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/756,366	01/14/2004	Hiroaki Nakano	TAI 146	2358

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RABIN & Berdo, PC
1101 14TH STREET, NW
SUITE 500
WASHINGTON, DC 20005

EXAMINER	
MAGEE, THOMAS J	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 10/28/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

14.D.

Office Action Summary	Application No.	Applicant(s)	
	10/756,366	NAKANO, HIROAKI	
	Examiner	Art Unit	
	Thomas J. Magee	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-15 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-15 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 01142004.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections – 35 U.S.C. 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1 – 4, 6, 7, 9 – 13, and 15 are rejected under 35 U.S. C. 102(e) as being anticipated by Lin et al. (US 6,534,852 B1).

3. Regarding Claim 1, Lin et al. disclose a circuit board/substrate (Col. 4, lines 17 – 20) for mounting a semiconductor chip, the circuit board including a semiconductor chip region (inside region 301) (Figure 3) for mounting the semiconductor chip and wiring regions (307, 309)

in which wirings (303) (Figure 6) are electrically connected to the semiconductor chip (Col. 4, lines 2 – 5),

the cicuit board/substrate comprising:

a reinforcement region (306) (Figure 3) in which reinforcement layers are formed for maintaining the strength of the circuit board for mounting the chip (Col. 4, lines 46 – 50), and

a protective film (302g) (Figure 5E) (Col. 6, lines 49 – 51) that covers the wirings,

wherein the wiring regions (307,309) (Figure 3) are disposed in a vicinity of the semiconductor chip region (301) and the reinforcement layer region (306) is disposed in the vicinity of the wiring regions.

4. Regarding Claim 2, Lin et al. disclose a circuit board/substrate for mounting a semiconductor chip, wherein the semiconductor chip (301) covers part of the wiring regions (See Figure 3).

5. Regarding Claim 3, Lin et al. disclose a circuit board/substrate for mounting a semiconductor chip, wherein the reinforcement layers (306) are copper wirings (Col. 4, lines 30 – 32).

6. Regarding Claims 4, 7, and 10, Lin et al. disclose a circuit board/substrate for mounting a semiconductor chip, wherein the protective film (302g) is flat and "planarized" (See Figure 5E).

7. Regarding Claim 6, Lin et al. disclose a method of manufacturing a circuit board for mounting a semiconductor chip, the circuit board including a semiconductor chip region (301) (Figure 3), a reinforcement layer region (306) in which reinforcement layers for maintaining the strength of the circuit board for mounting the semiconductor chip are formed, and wiring regions (307,309) in which wirings electrically connected to the semiconductor chip are formed (Col. 4, lines 2 – 5), the method comprising:

forming the wirings (307) in the vicinity of the semiconductor chip region (301),

forming the reinforcement layers (306) in the reinforcement layer region disposed in a vicinity of the wiring regions, and

forming a protective film (302g) (Figure 5E) (Col. 6, lines 49 – 51) that covers the wirings.

8. Regarding Claim 9, Lin et al. disclose a circuit board/substrate for mounting a semiconductor chip, the circuit board comprising:

an insulating substrate, the insulating substrate having a top surface and a bottom surface (Figure 6), with the top surface (Figure 3) including mutually separated first, second and third regions,

wirings (307,309) provided in the second region on the top surface of the insulating substrate, with the semiconductor chip being electrically connected to the wirings (Col. 4, lines 2 – 5),

reinforcement layers (306) provided in the the third region on the top surface of the insulating substrate, with reinforcement layers maintaining the strength of the circuit board for mounting a semiconductor chip (Col.4, lines 30 – 34),

a protective film (302g) formed on the insulating substrate so as to cover the wirings and reinforcement layers (Figure 5E),

the semiconductor chip (301) mounted on the protective film (302g) above the first region on the top surface of the insulating substrate,

wherein the third region (area around and laterally adjacent to chip mounting area, 301) encloses ("surrounds") the first and second regions.

9. Regarding Claim 11, Lin et al. disclose a circuit board/substrate for mounting a semiconductor chip, wherein the protective film (302g) is a solder resist (Col. 6, lines 49 – 51).

10. Regarding Claims 12 and 13, Lin et al. disclose a circuit board/substrate for mounting a semiconductor chip, wherein the reinforcement layers (306) comprise metal conductive layers (Col. 6, lines 39 – 42).

11. Regarding Claim 15, Lin et al. disclose a circuit board/substrate for mounting a semiconductor chip, further comprising solder balls (304) (Figure 6) that are disposed on the bottom surface of the insulating substrate and electrically connected to the wirings (Col. 4, lines 1 – 5).

Claim Rejections – 35 U.S.C. 103

12. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office Action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

13. Claims 5 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lin et al., as applied to Claims 1 – 4, 5 – 7, 9 – 13, and 15, and further in view of Norville (US5,407,615).

14. Regarding Claims 5 and 8, Lin et al. do not disclose the cutting and polishing of material form a protective film surface to attain planarization . Norville discloses a fine polishing technique for slow removal of material from plastic (polymer) surfaces (Col. 4, lines 34 – 38), wherein a polishing apparatus is used with varying grades of abrasive compounds. It would have been obvious to one of ordinary skill in the art at the time of the invention to combine

the polishing procedures of Norville with Lin et al. to attain flat planarized surfaces for mounting die within the package.

15. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lin et al., as applied to Claims 1 – 4, 5 – 7, 9 – 13, and 15, and further in view of Miyajima (US 6,365, 979 B1).

16. Regarding Claim 14, Lin et al. do not disclose that the reinforcement layers comprise insulating materials. Miyajima discloses a substrate wherein a two layer solder resist protrusion is formed (4,5) (Figure 4C) at the lateral edges of the chip surrounding the wiring pads (2a) with the protrusion acting as a protective layer and a strength reinforcement layer (Col. 3, lines 36 – 44). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine Miyajima and Lin et al. to obtain a package with reduced field coupling in the housing.

Conclusions

17. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to **Thomas Magee**, whose telephone number is **(571) 272 1658.** The Examiner can normally be reached on Monday through Friday from 8:30AM to 5:00PM (EST). If attempts to reach the Examiner by telephone are unsuccessful, the examiner's supervisor, **Eddie Lee**, can be reached on **(571) 272-1732.** The fax number for the organization where this application or proceeding is assigned is **(703) 872-9306.**

Thomas Magee
October 20, 2004

EDDIE LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800